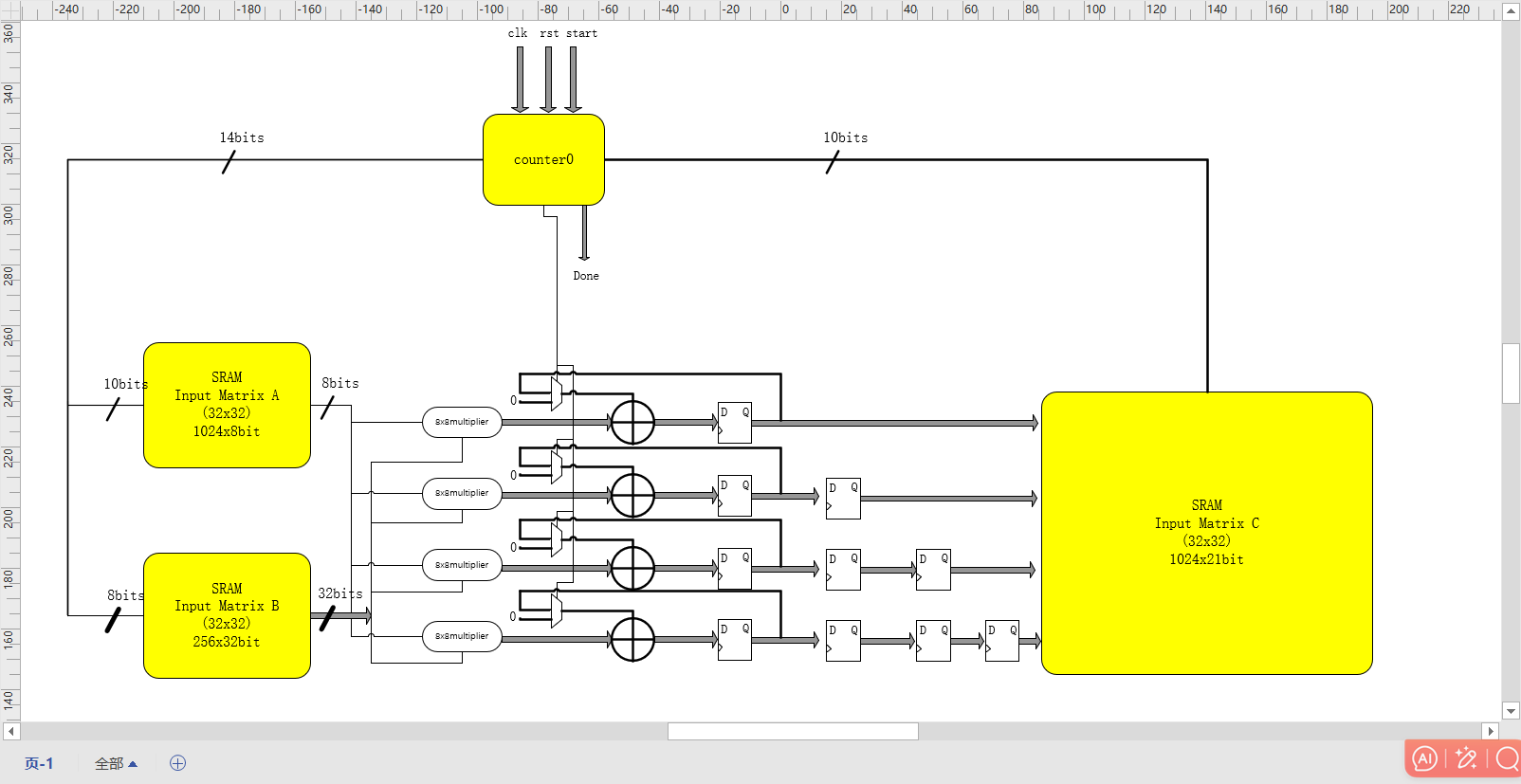
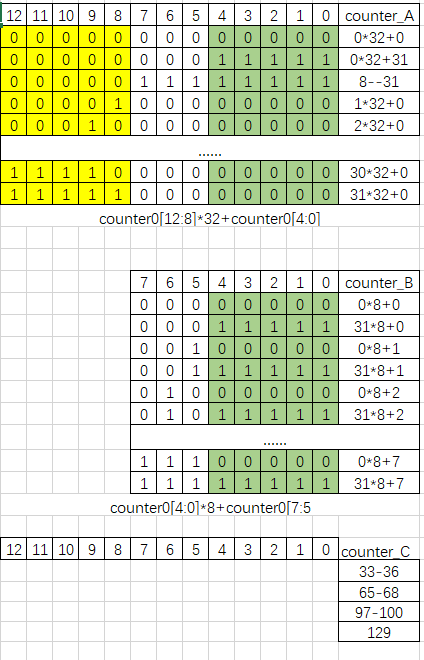
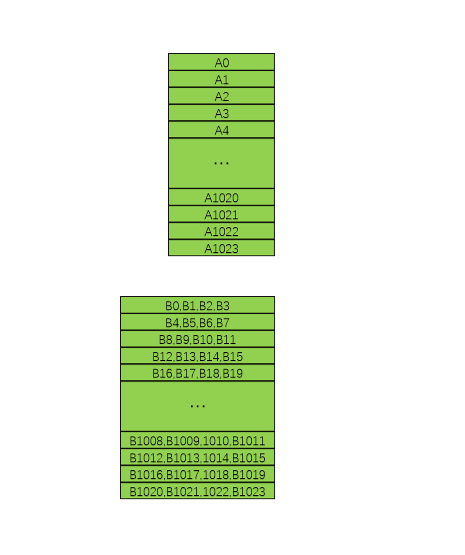
**Project 1**

1. Circuit diagram:

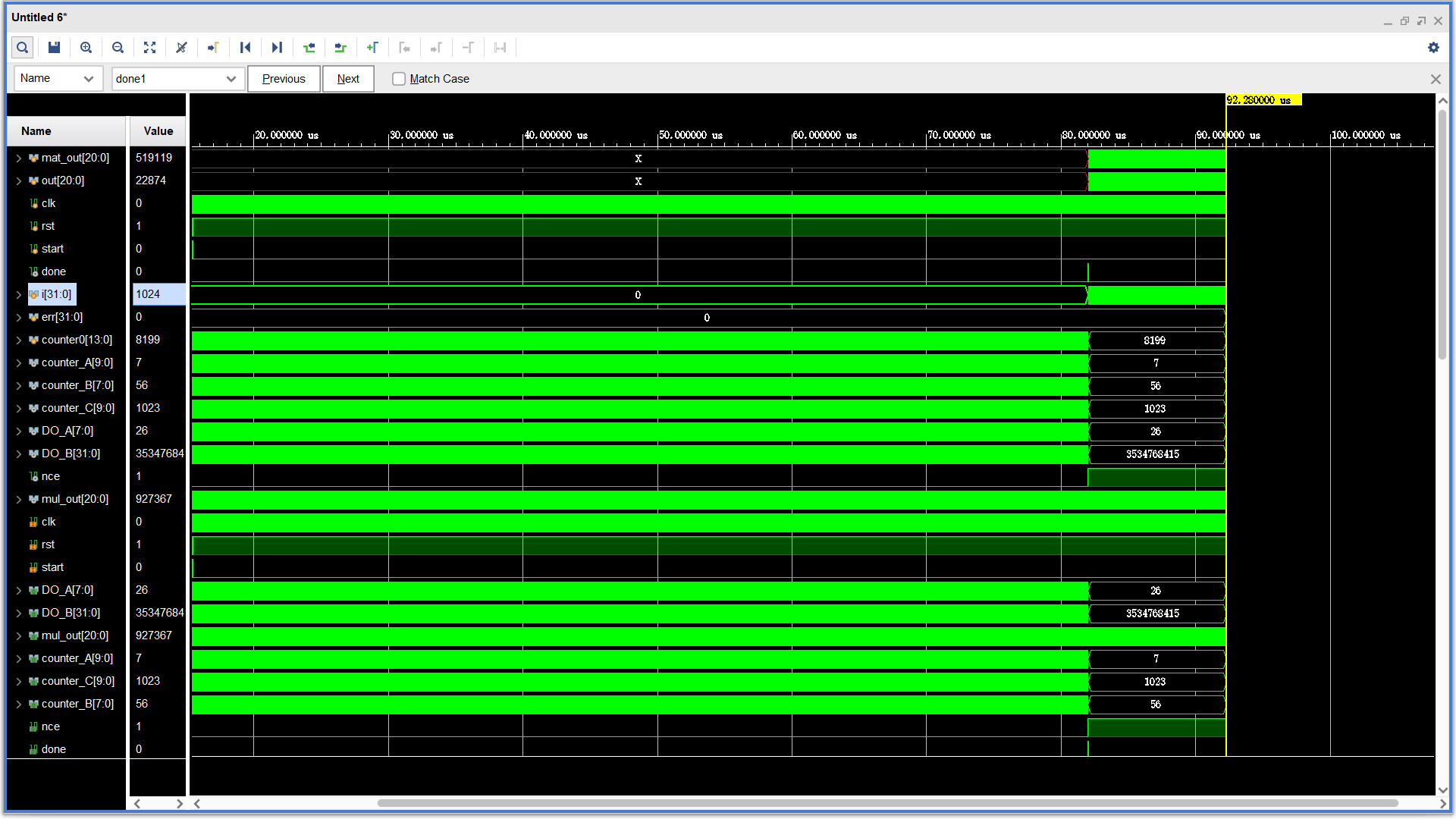


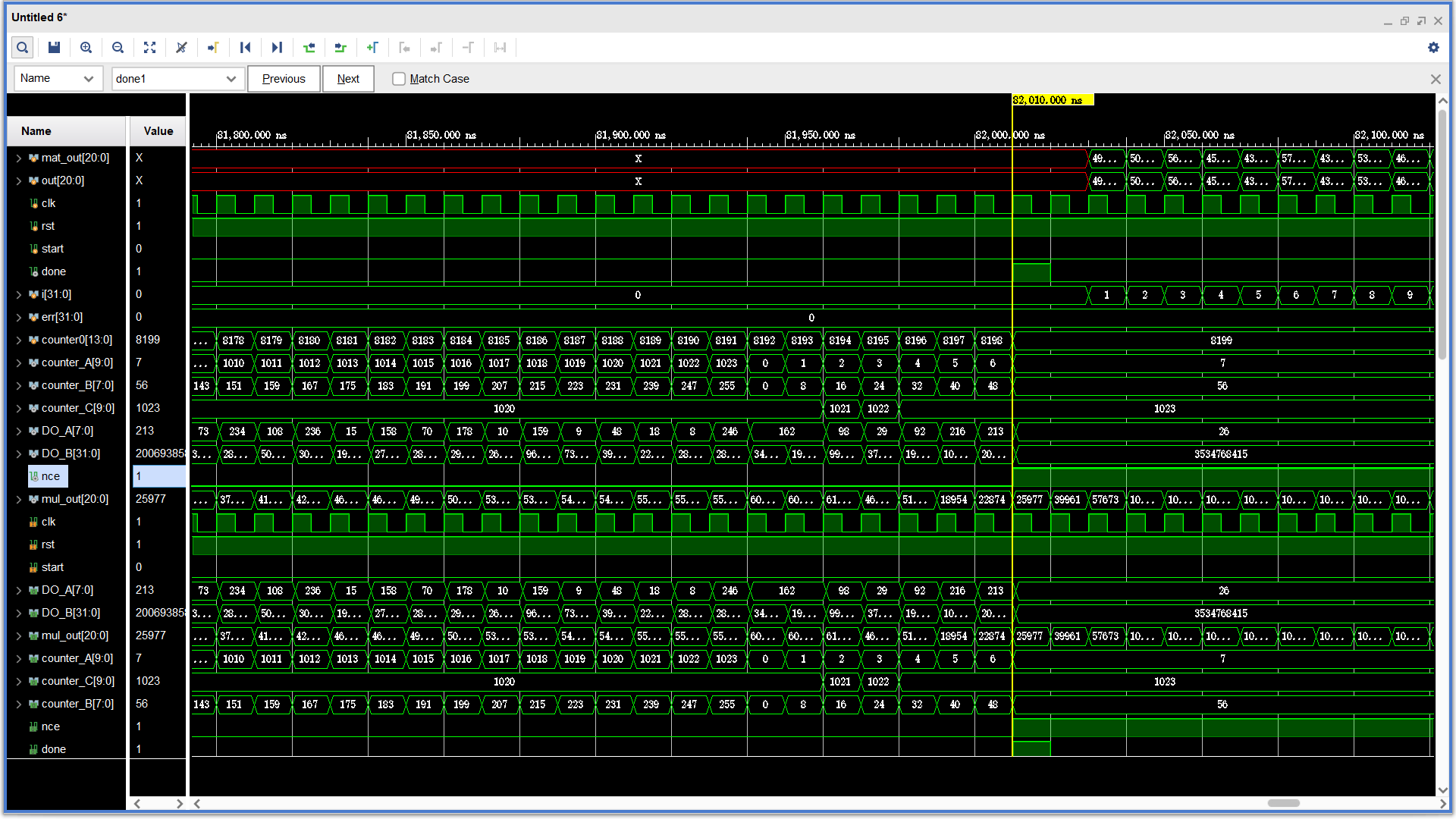
From the block diagram, counter0 will increase as the start signal is initiated. The nce signal is set to 0 simultaneously. The address bits for SRAM A, counter\_A, are 0, 1, 2...31, and they cycle through these 32 times. Then it progresses from 32 to 63, cycling through 32 times, and continues in this pattern until counter\_A reaches 992~1023, cycling through 32 times. The address bits for SRAM B, counter\_B, start at 0, 8, 16...248, then move to 1, 9, 17...249, and continue adding in this manner, executing 32 times, then cycling through 32 times. The address bits for SRAM C, counter\_C, need to wait 32 cycles after the start signal before they can increment by 1, and can only do so four times, because the four results from multiplication need to be stored in SRAM C. When counter0 equals 5'b00001, it signifies a new computation, hence the output of the mux is 0, and in all other cases, the output is the cumulative value. Therefore, every 32 cycles, the four computed values are stored in SRAM\_C. We can observe the following relationships between counter\_A, counter\_B, counter\_C, and counter0:

The data Do\_A,Do\_B is stored in memory like this:



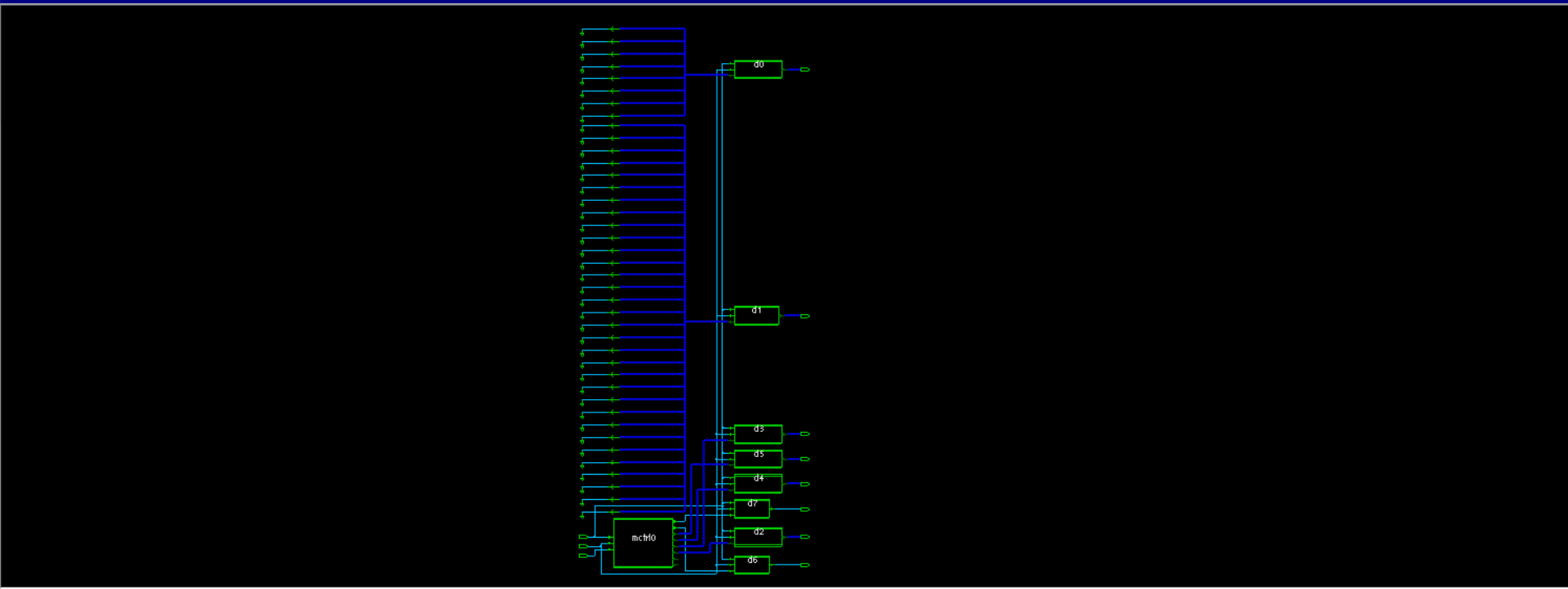
1. Timing diagram:

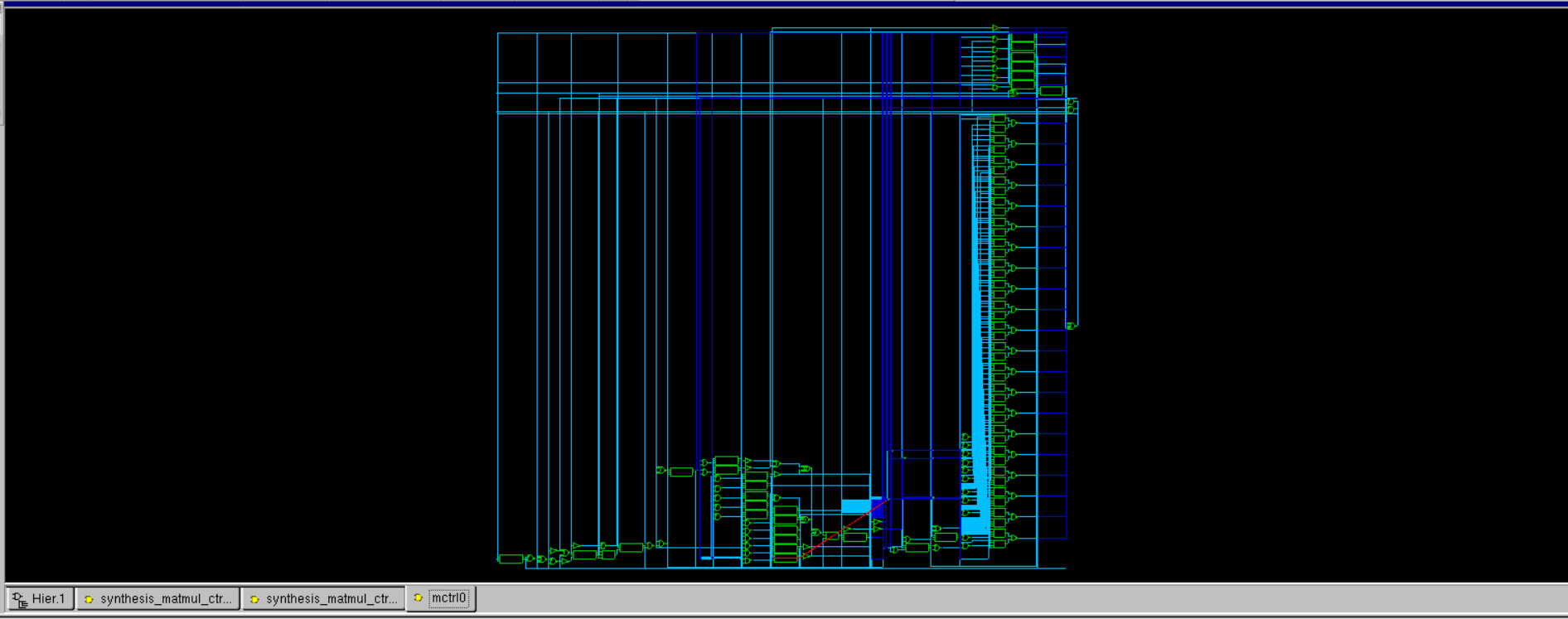




After the 'done' signal becomes 1, the matrix computation is completed. The 'nec' signal becomes 1, disabling counter0 and memory modules A, B, and C. The error is zero, it indicates that the coding and simulation results are correct.

3.Schematic

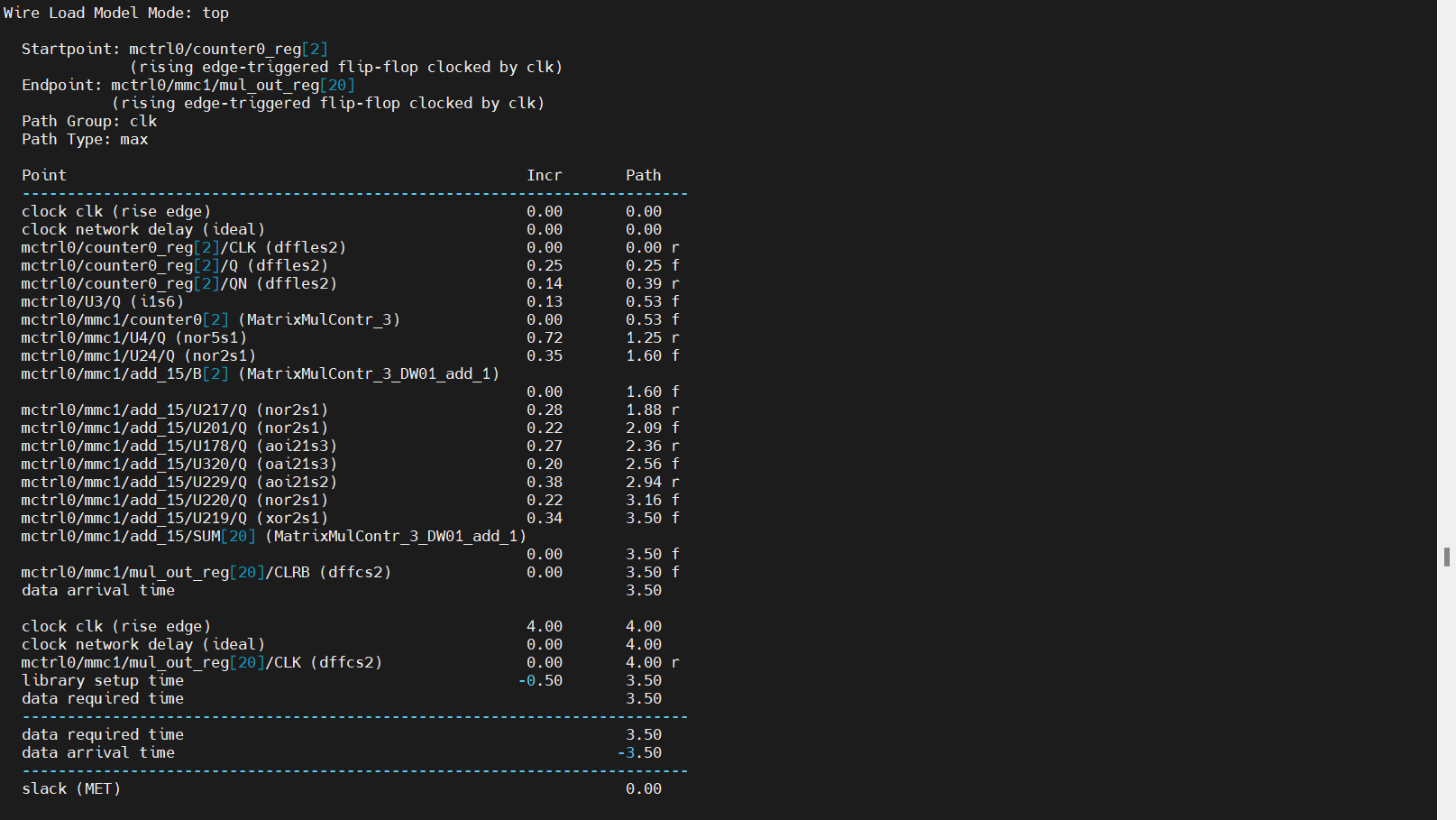




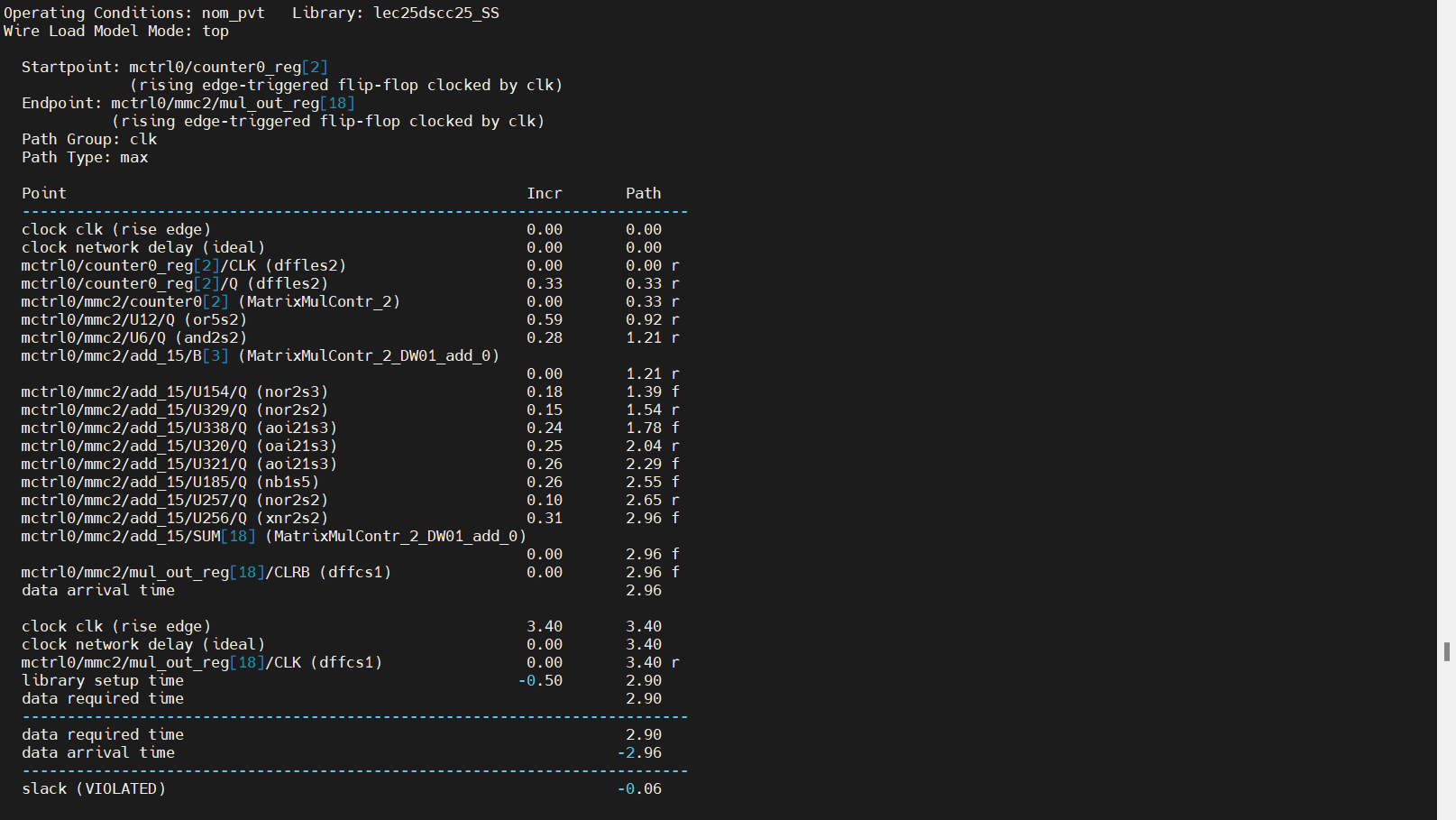
The delays are primarily from the Matrix Multiplication Controller module. To check the critical path, note that the delays mainly originate from the 8-bit multiplier, adder, and counter0.

4.Area,timing and power

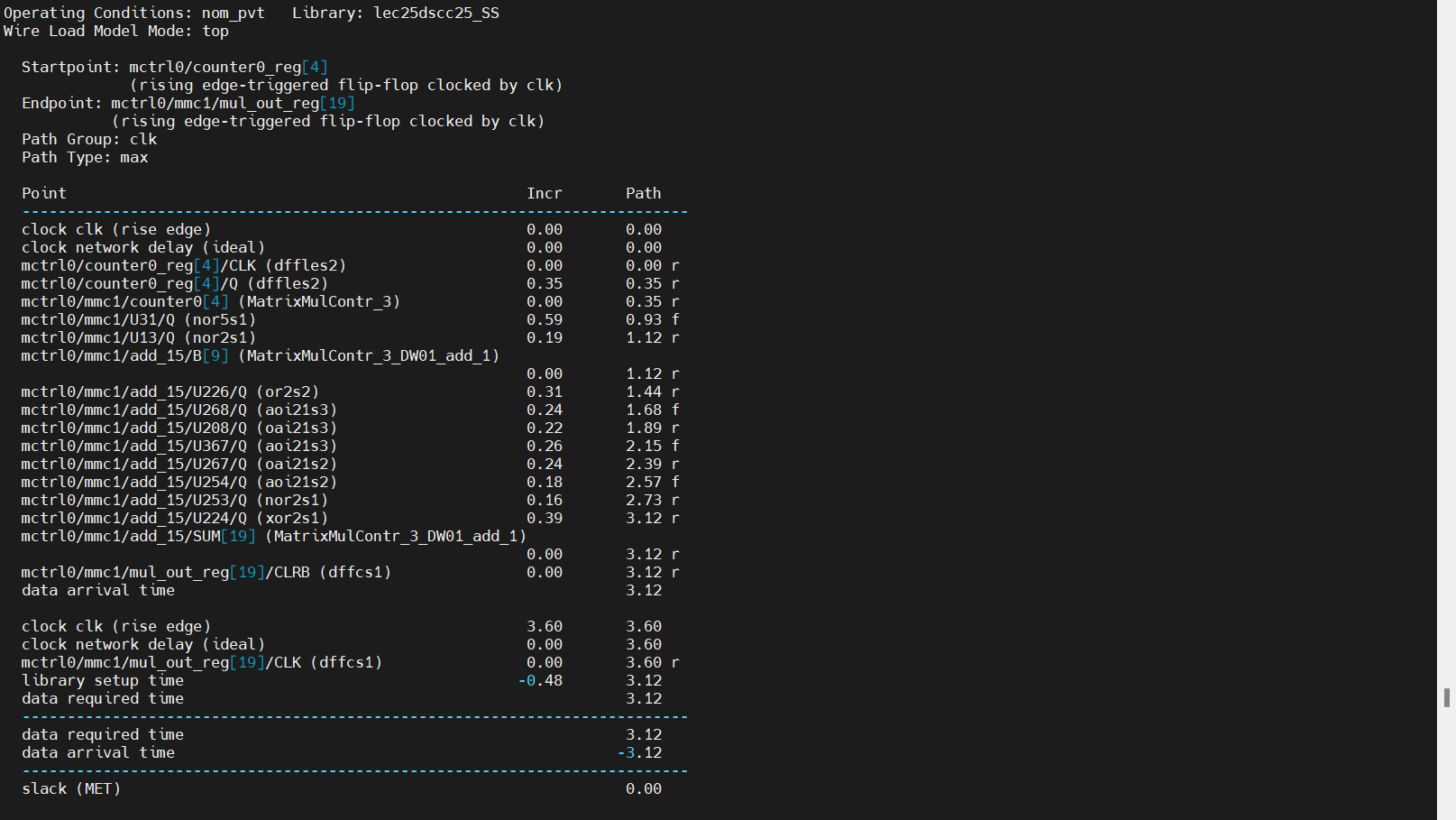
T=4ns:



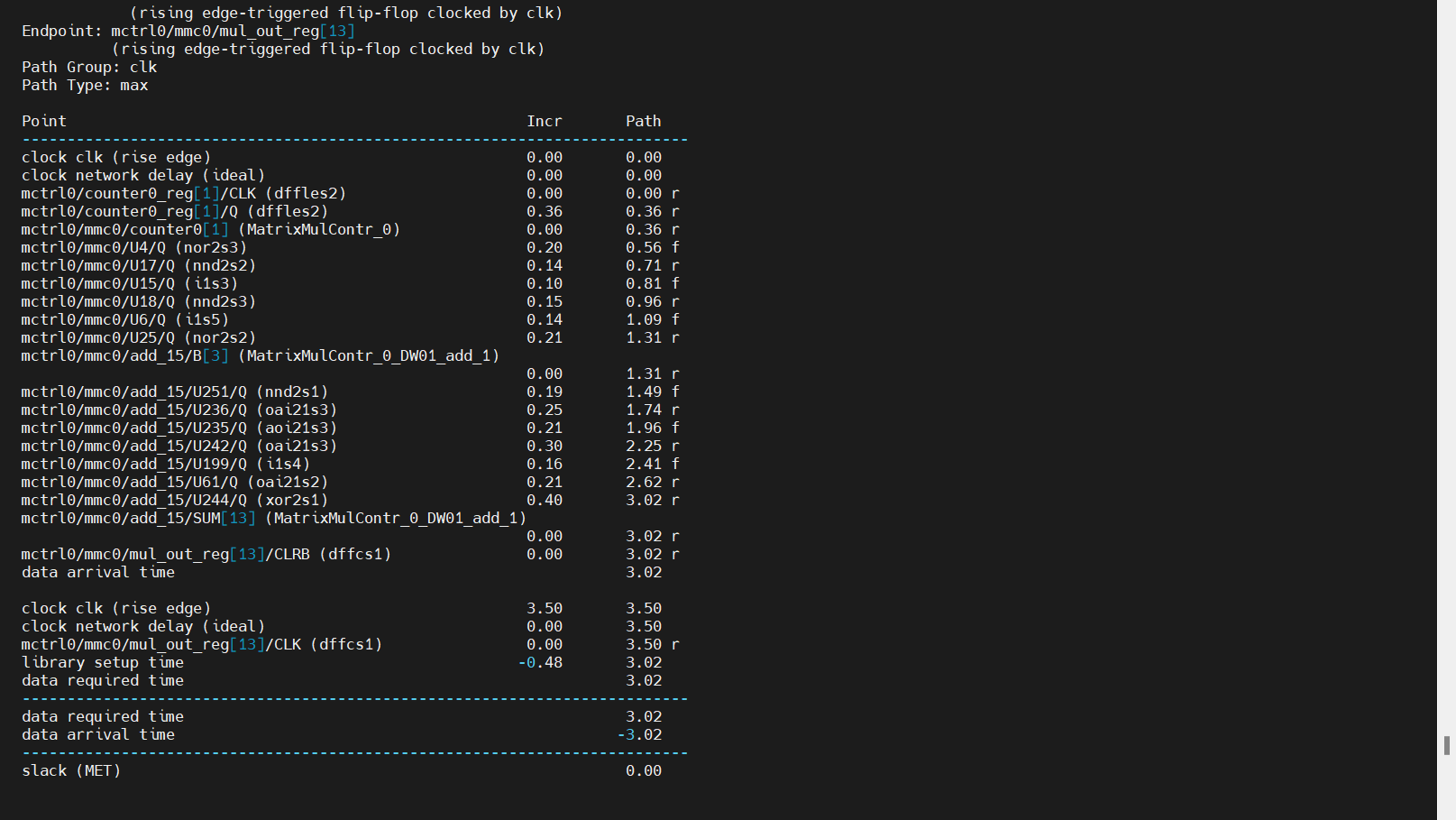
T=3.4ns:



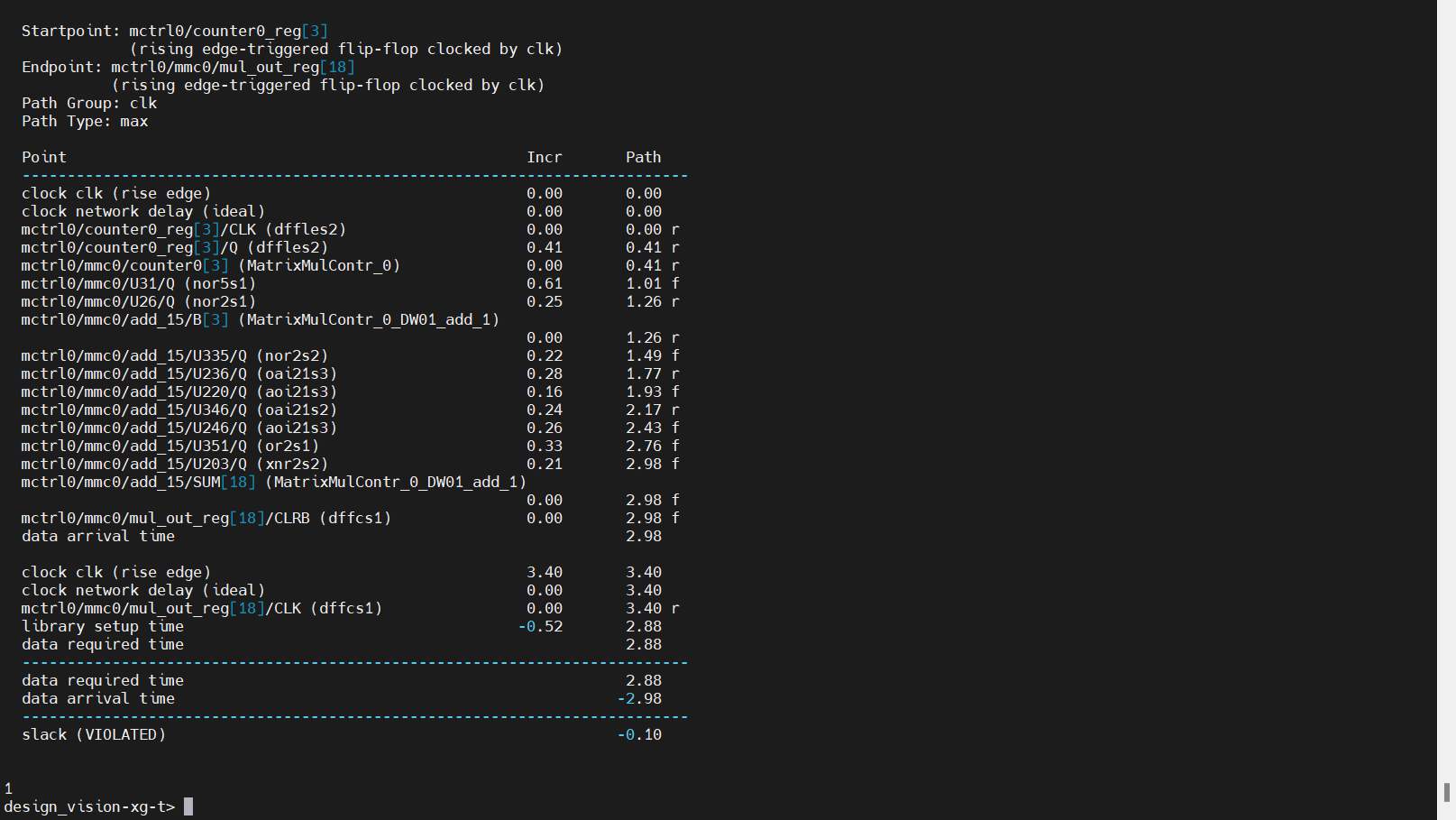
T=3.6ns:



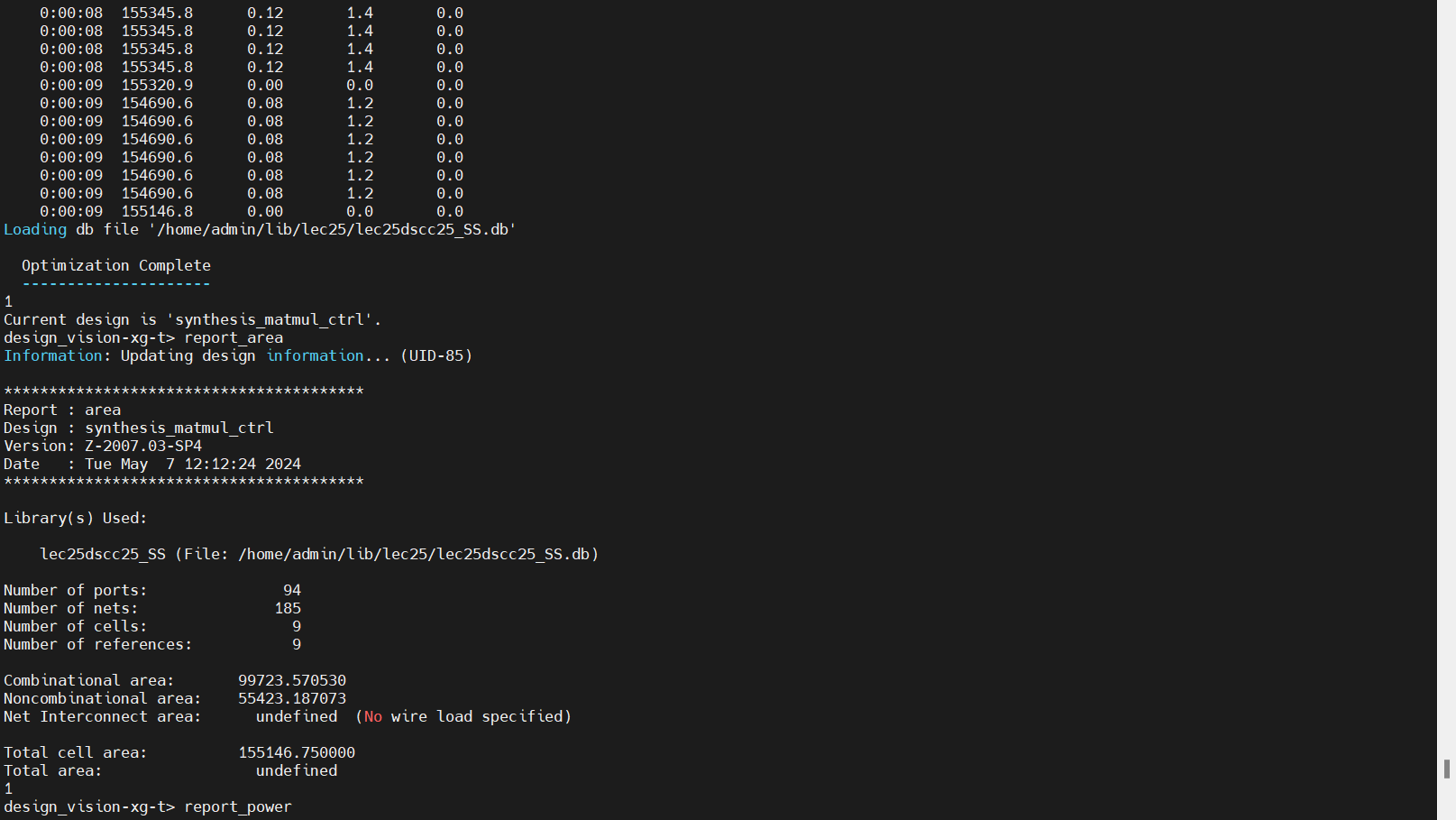
T=3.5ns



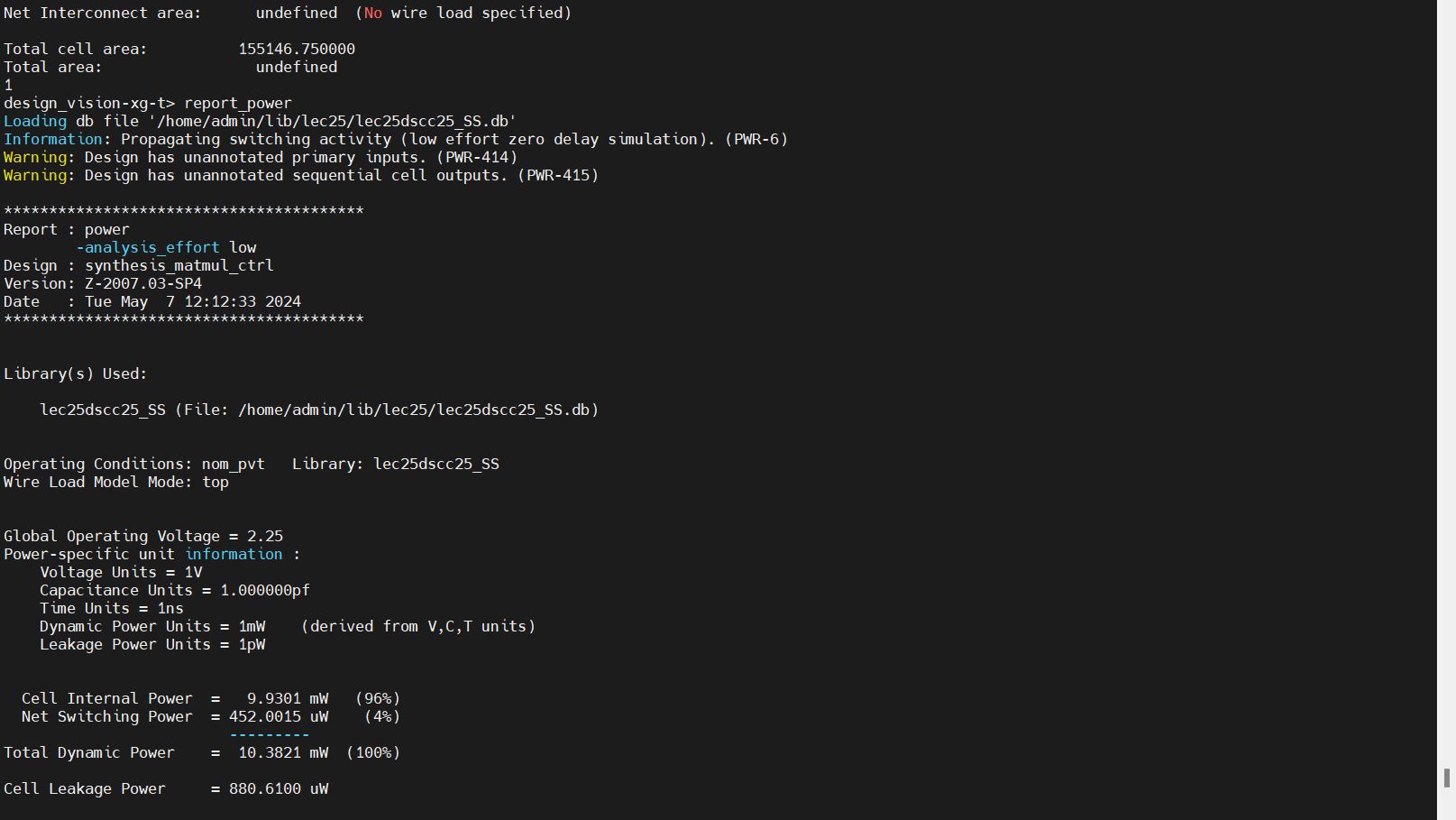
T=3.4ns:



Area:



Power:



The maximum clock period is 3.5 ns, equivalent to 285.7 MHz. Combinational area: 99,723.570530; Non-combinational area: 55,423.187073. The area is very large because there are four Computation Units in the Matrix Multiplication Controller. This design focuses on matrix calculations, requiring a 32x32x32 multiplication process. Therefore, the power consumption is also significant.

5.Concusion

In this design, the most important component is the counter, as it controls the addresses of memories A, B, and C. The addresses of these memories will increase according to the Matrix Multiplication Controller. The design indicates that the clock period will decrease as the throughput increases, but the area will increase. To reduce power consumption, the 'done' signal will change to 1 immediately after the multiplication is finished, and then revert to 0 after one clock cycle.